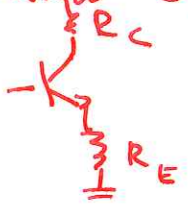
BJT Golden Rules

1) $I_E = I_C$ (ok: $I_E = I_C + I_B$ but generally $I_C \gg I_B$ in fact (see below) $I_C = \beta I_B \Rightarrow I_E = (\beta+1) I_B$)

$V_B = V_E + .6$ (ok: the 'turn-on' voltage of a forward biased PN junction varies with temperature & large I_B does mean larger V_{BE} but during normal operation V_{BE} typically varies only $\pm \frac{1}{40}$ V — small change)

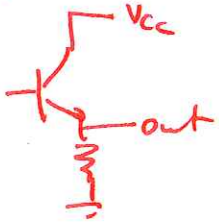
Common Emitter Amp



$\Delta I_E = \frac{\Delta V_B}{R_E}$

$\Delta V_{out} = -R_C \Delta I_C = -\frac{R_C}{R_E} \Delta V_B$

Emitter Follower

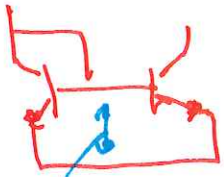


$\Delta V_{out} = \Delta V_B$

2) $I_C = \beta I_B$ (but: range of β allowed by specs large. β Not constant — varies with I_B)

Avoid circuits that depend on a particular value of β — they may not work with replacement transistor.

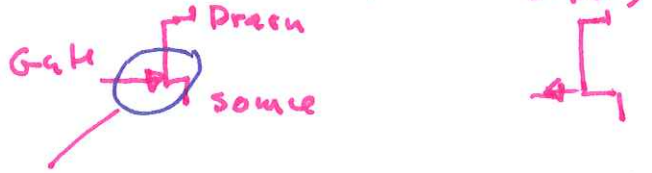
3) I_B, I_C in fact functions of V_{BE} — match V_{BE} match results. (For a "matched pair")



same V_{BE} - same currents thru device.

FETs vs Bipolar Junction Transistors

2 basic types: n-channel & p-channel
- n-channel → positive supply
- p-channel → negative supply



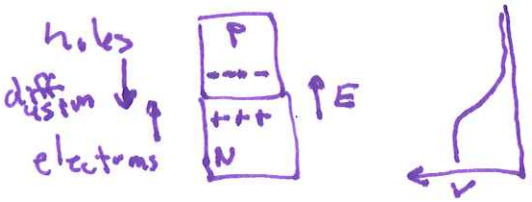
the controlling terminal is a PN junction: diode

Back Biased Diode
therefore intrinsic high input impedance

2 basic types: NPN & PNP
- NPN → positive supply
- PNP → negative supply

the controlling terminal is a PN junction: diode

Forward Biased Diode
therefore intrinsic low input impedance



As electrons / holes diffuse & combine in "foreign" soil charge layers build up near junction. Eventually the resulting $\vec{E}$ is large enough to stop further diffusion (dynamic equilibrium)

The resulting V barrier literally keeps a lid on diffusion — change that barrier & expo more current flows: $\propto e^{e\Delta V/kT} \Rightarrow I \approx I_0 e^{\Delta V/V_T}$ ← $V_T = \frac{kT}{e} \approx \frac{1}{40}\,V$

$$\frac{dI}{dV} \equiv \frac{1}{r} = \frac{1}{V_T} I_0 e^{V/V_T} = \frac{I}{V_T} \Rightarrow r = \frac{V_T}{I} = \frac{1000\,V_T}{I(mA)}$$

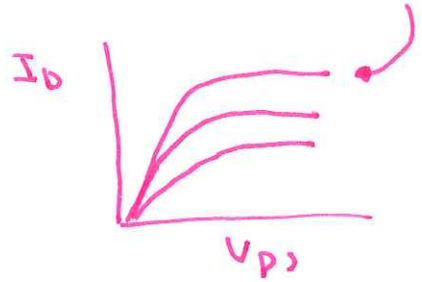
($\frac{I(mA)}{1000}$)

r: ac resistance

$$= \frac{25}{I(mA)}\ \Omega$$

"engineering 8"

The characteristic curves are labelled with gate voltage



plateaus are spaced quadratically $I_D \propto (V_{GS} - V_T)^2$

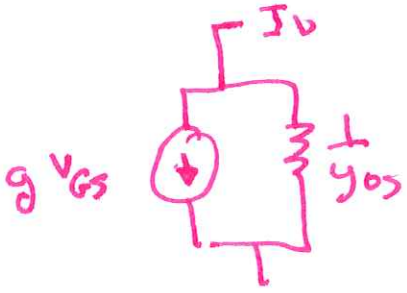
AC behavior (Taylor Expansion)

$I_D(V_{DS}, V_{GS})$

$$dI_D = \frac{\partial I_D}{\partial V_{DS}} dV_{DS} + \frac{\partial I_D}{\partial V_{GS}} dV_{GS}$$

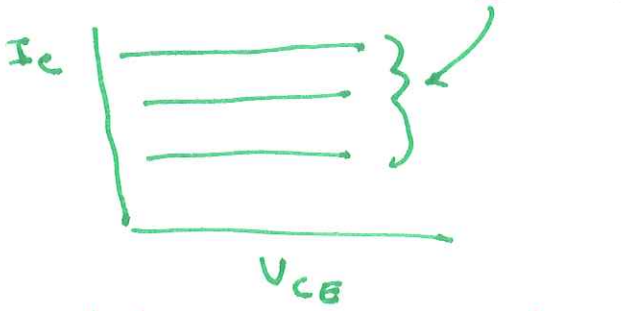
$\frac{\partial I_D}{\partial V_{DS}} = y_{OS}$ $\quad$ $\frac{\partial I_D}{\partial V_{GS}} = y_{FS} = g$

admittance



"saturated" = active region where I_D plateaus

The characteristic curves are labelled with base current



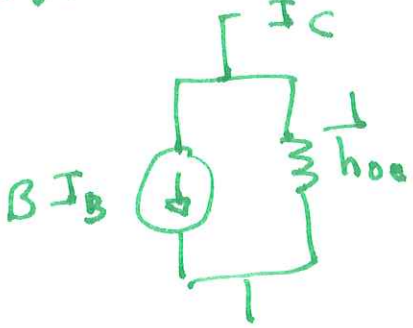
plateaus are spaced linearly $I_C \propto I_B$

$I_C(V_{CE}, I_B)$

$$dI_C = \frac{\partial I_C}{\partial V_{CE}} dV_{CE} + \frac{\partial I_C}{\partial I_B} dI_B$$

$\frac{\partial I_C}{\partial V_{CE}} = h_{OE}$ $\quad$ $\frac{\partial I_C}{\partial I_B} = h_{FE} = \beta$

hybrid



"saturated" = region where V_{CE} is small — same approx location as "linear region" in FET

The gate draws essentially zero current: $I = I_0(e^{V/V_T} - 1)$, with $e^{V/V_T} \approx 0$

So DC corresponds to high Z; AC corresponds to capacitor.

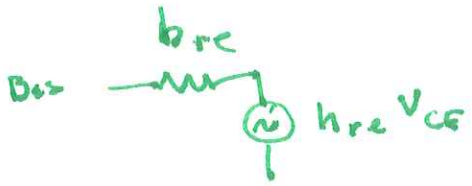
The base must draw current to be in active region & hence ~kΩ DC $\left[r = \frac{25\Omega}{I_B(mA)} \right]$; AC

there are "stray capacitance" to both emitter & collector but we will largely ignore these.

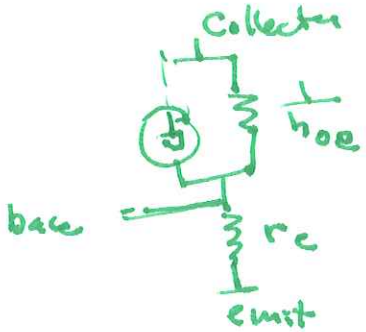
$$dV_{BE} = \frac{\partial V_{BE}}{\partial V_{CE}} dV_{CE} + \frac{\partial V_{BE}}{\partial I_B} dI_B$$

$\frac{\partial V_{BE}}{\partial V_{CE}}$: $h_{re} \sim 10^{-4}$, often ignored

$\frac{\partial V_{BE}}{\partial I_B}$: h_{ie} (unit Ω $\simeq \frac{25\Omega}{I_B(mA)}$)



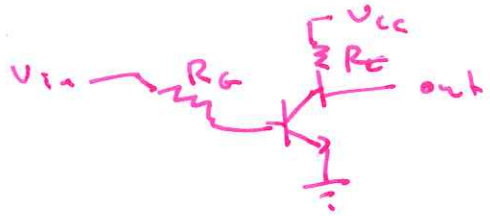
REMARK: Hit thinks of input base resistor as actually connected to emitter:



re is smaller than h_{ie} (current $I_C + I_B$ flows through it) but its voltage effect on base is multiplied by (β+1) so net result is exactly as h_{ie}.

Thinking about it as if an emitter allows it to be combined with actual emitter resistors to make nicer formulas

Do Not Build this Circuit! (theory only)



since $V_{Base} = .6\ V$ (fixed)

$$\Delta I_B = \frac{\Delta V_{in}}{R_G}$$

$$\Delta I_C = \beta\, \Delta I_B$$

$$\Delta V_{out} = -R_C\, \Delta I_C$$

$$= \frac{-R_C}{R_G}\, \beta\, \Delta V_{in}$$

→ voltage gain A_v

$$A_v = \frac{-R_C}{R_G}\, \beta$$

There are several things wrong with this analysis

Note $A_v = \infty$ is implied if $R_G \to 0$

you will show eventually max A_v of this circuit is $20 \times V_{cc}$

[of course you know going for max gain is a mistake — throw away that gain with negative feedback to improve circuit performance]