Some History

1906 - triode vacuum tubes
de Forrest

1912-20 - rise of radio
based on vacuum tubes

WW II: radar / magnetron
"Rad Lab" at MIT

1947 - Bell Labs
contact transistor
Bardeen, Brattain
Shockley

1948 - BJT

1959 - MOSFET

1959 - Jack Kilby (TI)
Bob Noyce (Fairchild)
Integrated Circuit

1957 - "traitorous eight"
leave Shockley for
Fairchild - eventually
forming Intel in
1968 - Gordon
Moore

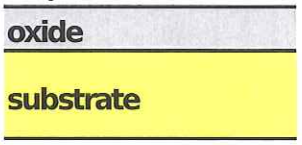
1971 4 bit microprocessor
Intel 4004
TI TMS1000

1974 - 8 bit microprocessor

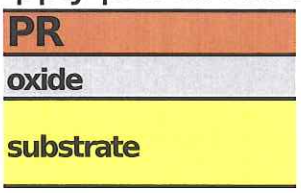
1979 - Intel 8086

From Wiki: "photolithography":

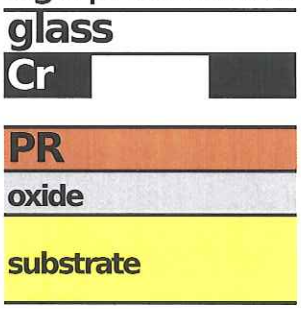
a. Prepare wafer



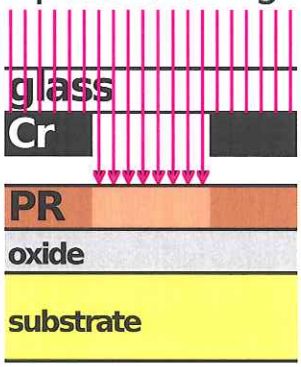
b. Apply photoresist



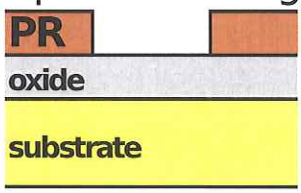
c. Align photomask



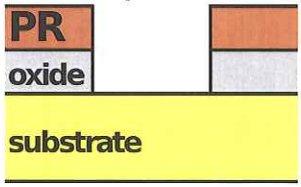
d. Expose to UV light



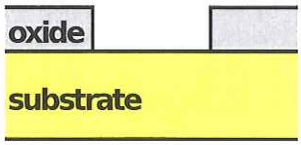
e. Develop and remove photoresist exposed to UV light



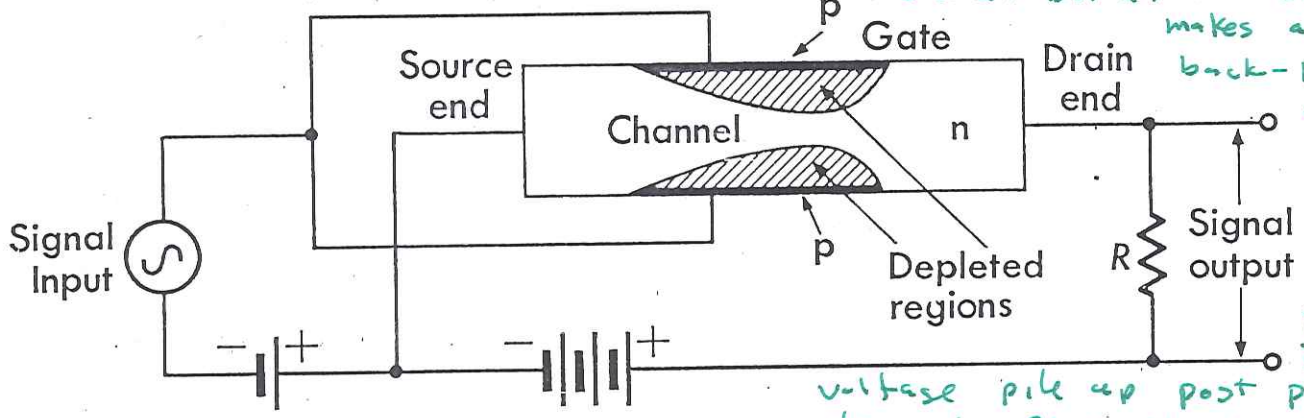
f. Etch exposed oxide



g. Remove remaining photoresist

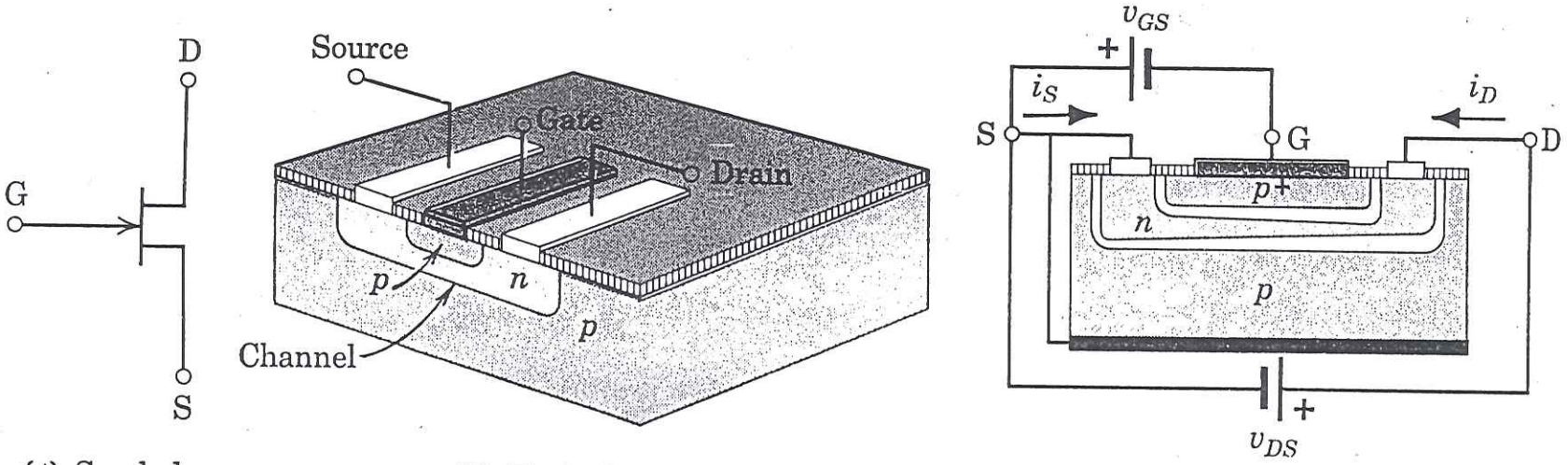


Integrated circuits are built up/ carved out as a series of planes. The features of the plane are defined by light shining thru a mask; "photo resist" plays the role of the film - where exposed to light & "developed" the layer below is exposed & may be acted on (carved out, built up) Many such layers are required. The smallest feature size is determined by the wavelength of the light used - UV & high n materials yield shorter λ.



An increasingly positive drain voltage trys to increasingly "suck" electrons from the source. But at the same time this makes an increasingly back-biased PN junction with the gate — the depletion regim grows & the channel restricts. when it closes further increases in gate voltage pile up post pinch off and do not affect the input flow — FD

FIG. 3.30. Schematic representation of a field-effect transistor. "Saturday"



(a) Symbol (b) Typical structure (c) Channel depletion

Figure 6.1 An *n*-channel depletion-mode field-effect transistor (JFET).

← enhancement mode MOSFET – we make the n channel in p-type material and then pinch it off

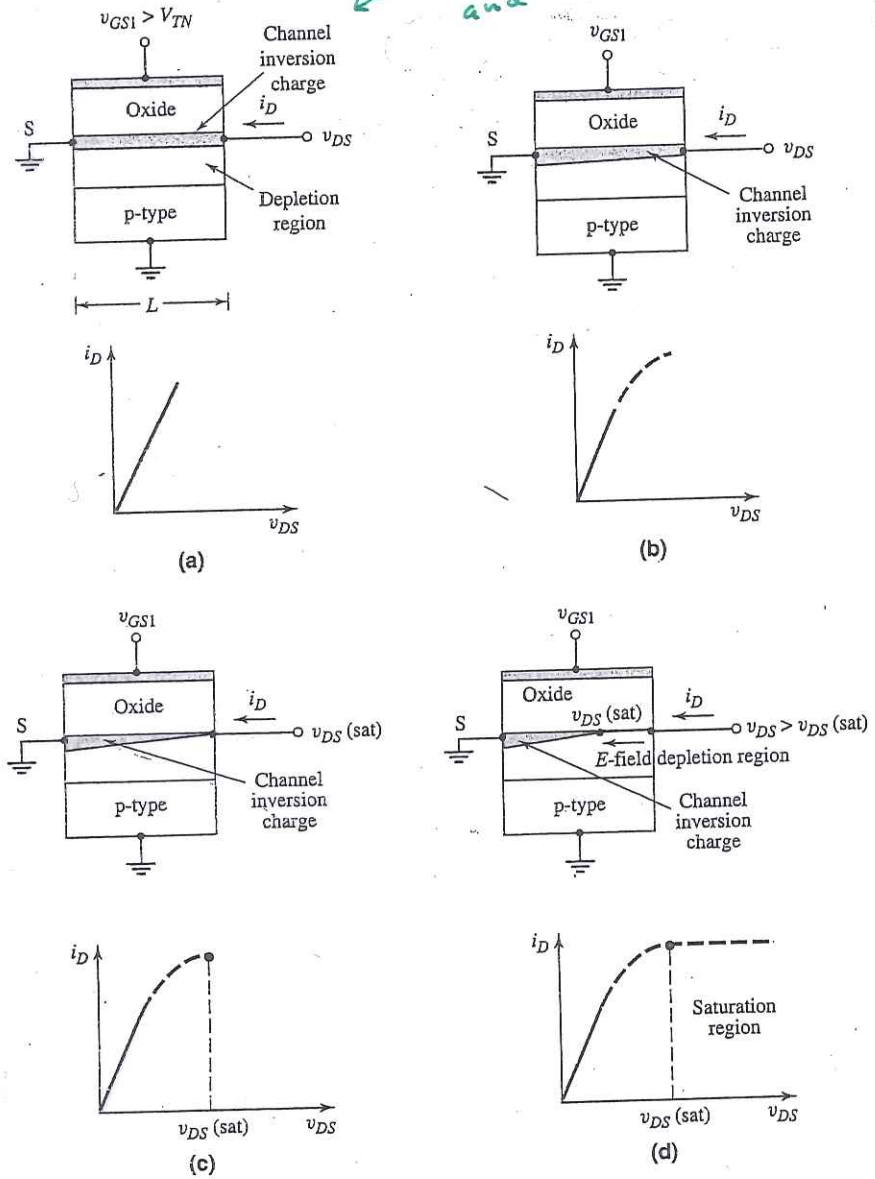


Figure 3.9 Cross section and i_D versus v_{DS} curve for an n-channel enhancement-m MOSFET when $v_{GS} > V_{TN}$ for (a) a small v_{DS} value, (b) a larger v_{DS} value but for $v_{DS} < v_{DS}(\text{sat})$, (c) $v_{DS} = v_{DS}(\text{sat})$, and (d) $v_{DS} > v_{DS}(\text{sat})$

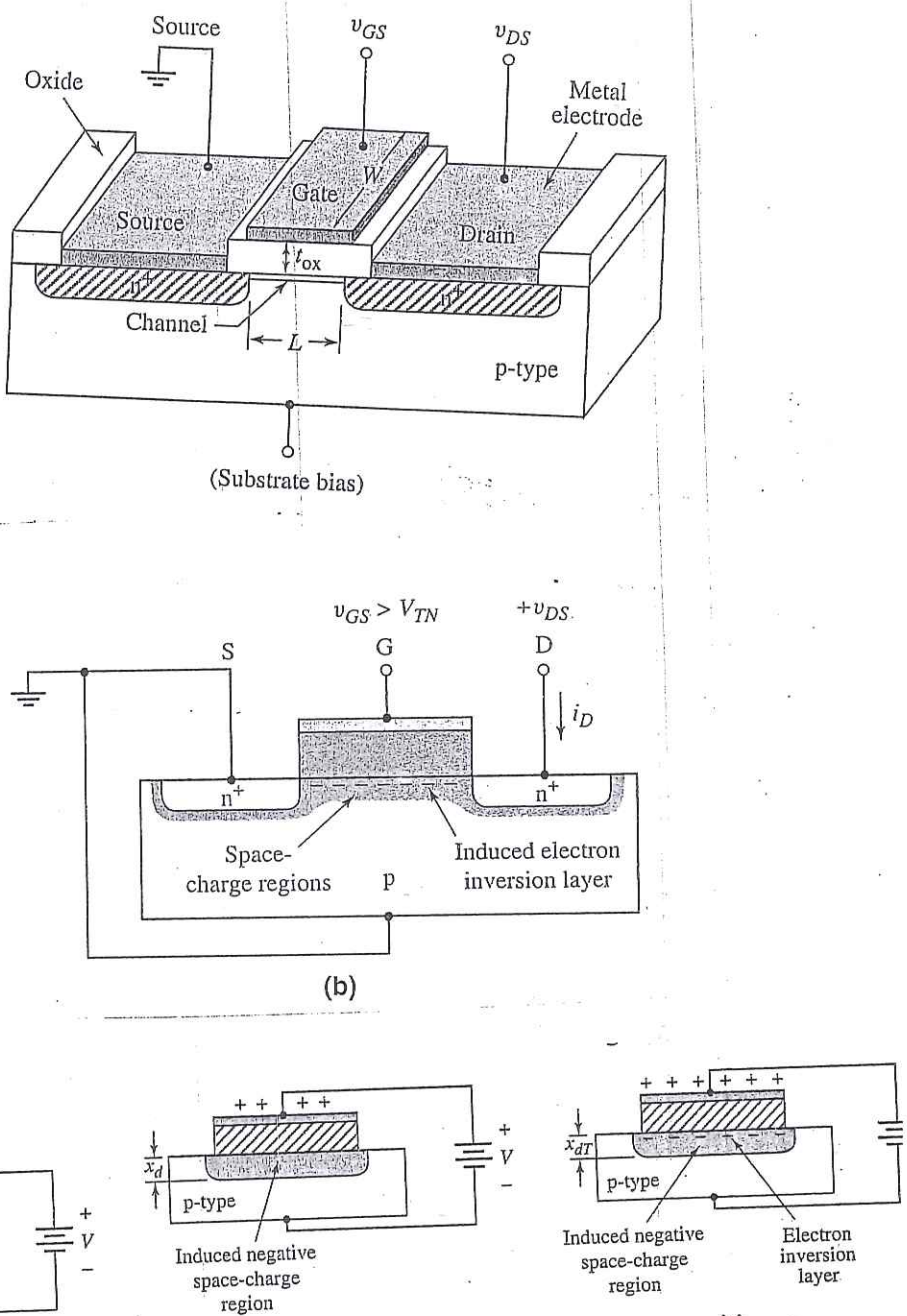


Figure 3.3 The MOS capacitor with p-type substrate: (a) effect of positive gate bias, showing the electric field and charge flow, (b) the MOS capacitor with an induced space-charge region due to a moderate positive gate bias, and (c) the MOS capacitor with an