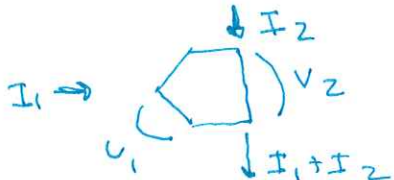


Small Signal Model — the superposition theorem allows us to totally separate signals at different frequencies. In particular we separate the DC signals (volt/amps) — which we call the 'bias' — from AC signals. We must assume the AC signals are 'small' so we can approximate non-linear response with just the linear term of Taylor approx. [Superposition requires linear circuit elements]

Thus we consider a generic 3-terminal device



We assume currents are known functions of voltages. [There is nothing special about this — in future we'll consider cases where voltage is a function of current. On the other hand the range of validity of Taylor Approx may depend on what we take as dependent / independent variables — i.e. some models really are better than others]

$$I_2(V_1, V_2) : dI_2 = \frac{\partial I_2}{\partial V_1} dV_1 + \frac{\partial I_2}{\partial V_2} dV_2$$

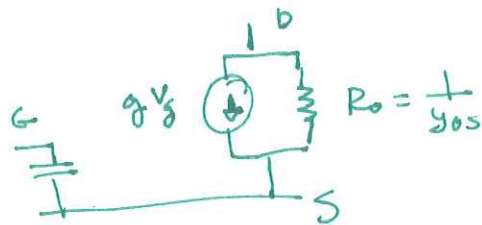
transconductance g
 forward admittance Y_{fs} output admittance $Y_{os} = \frac{1}{R_o}$

$$I_1(V_1, V_2) : dI_1 = \frac{\partial I_1}{\partial V_1} dV_1 + \frac{\partial I_1}{\partial V_2} dV_2$$

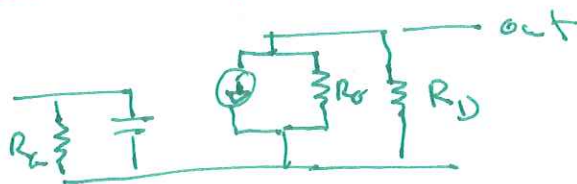
input admittance $Y_{is} = \frac{1}{R_i}$ so small I_{bias} never seen a value for this

For FETS this term is truly small, bias dependant and hence not in spec sheet
 Note: input capacitance is in spec sheet $\rightarrow Y_{os} = i\omega C$

Roaltray model for FET:



AC model for common source amp:



so gain is now $g(R_o || R_D)$

EE notation (which I will probably violate sometimes)

I_D - DC current into drain - **cap symbol & subscript**

i_d - AC current into drain - **lowercase " "**

i_D - AC+DC current into drain - **lowercase symbol uppercase subscript**

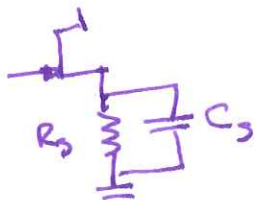
eg (future) h_{FE} - ratio of 2 total currents

h_{fe} - ratio of just AC parts

Remark: Common Source Amp - rid $\frac{1}{L} V_G \dot{=} \frac{1}{R_g}$ (maybe)

plan: have $V_G = 0V$ but $V_S = +1V$ (eg) so

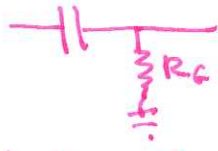
$V_{GS} = -1V$. Let V_S be steady even as I_S (i_s) varies.



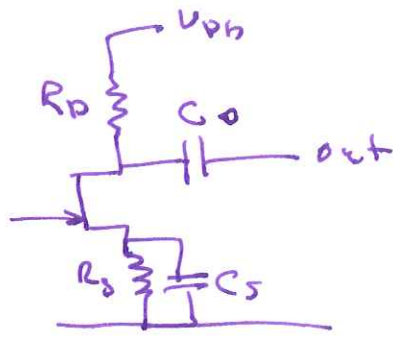
select $R_S \Rightarrow I_D R_S = \text{desired } |V_{GS}|$

select $C_S \Rightarrow \frac{1}{\omega C} \ll R_S$ for lowest desired freq.

Design



high pass filter
blocking cap



Select Q-point (aka operating point)

$$\rightarrow V_{DS} \approx \frac{V_{DD}}{2}$$

\rightarrow smaller $I_D \rightarrow$ bigger R_D

\Rightarrow bigger gain

but bigger output impedance

Given an operating point - Find R_D/C_S to supply the required bias

C_0 : This cap will probably be connected to something with an R_{in} . Good practice requires that R_{in} to be big compared to circuit's output impedance ($= R_D \parallel \frac{1}{g_{m3}}$) ; generally $R_D \ll \frac{1}{g_{m3}}$.

Thus we should be ok with $X_C = R_D$

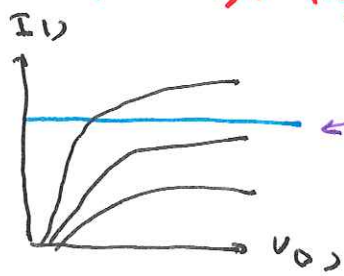
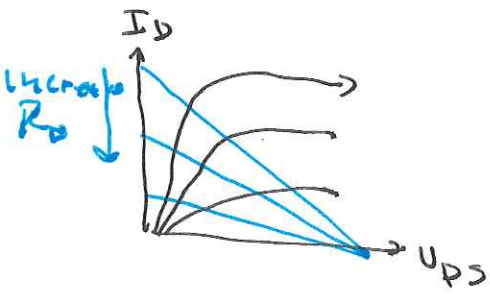
[Solve for C using lowest interesting freq]

Additional FET circuits.

Note that for common source amp, if we went for higher gain by increasing R_D the operating point was pushed to closer to V_T with resulting reduction in g .

[increasing R_D does result in higher gain - just not as much gain increase as might expect]

Warning: this idea of going for increased gain is almost always the wrong approach - eg it increases Z_{out} which is generally bad. We introduce it here mostly as a way of introducing the idea of an "active load" - not because its anything to actually do.

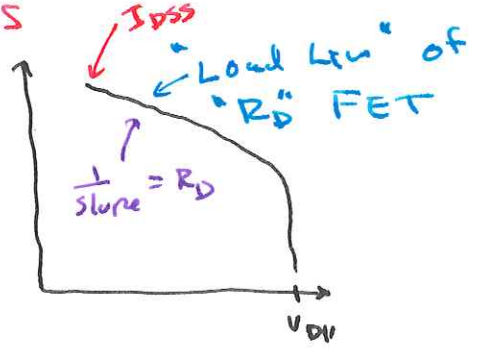
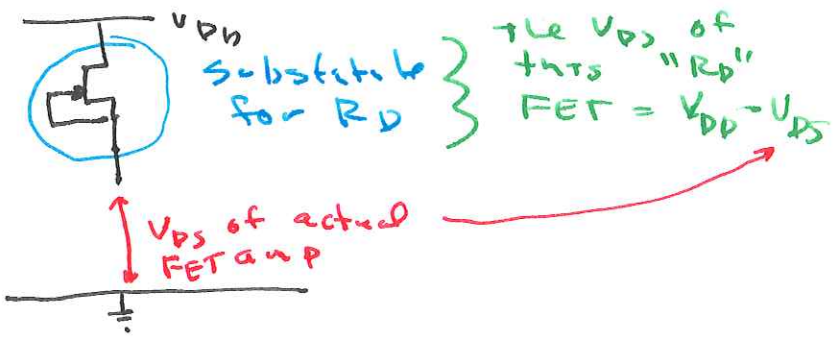


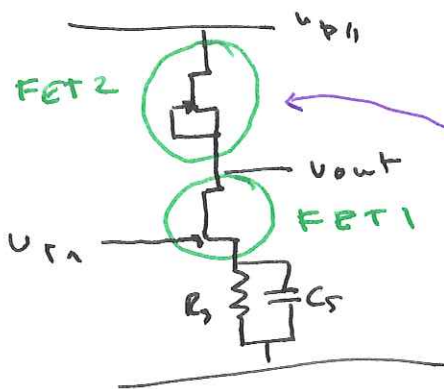
if we had a load like this very small changes in V_G → big V_{DS} swings i.e. big gain

a device like this would be called a constant current source.

Remark 1: since the slope on I_D vs V is $\frac{1}{R}$, constant current sources correspond to $R = \infty$ [Note $R_D \rightarrow \infty$ should give use big gain as $A \approx -g R_D$]

Remark 2: (Important) A FET acts a bit like a constant current source - i.e. those plateaus

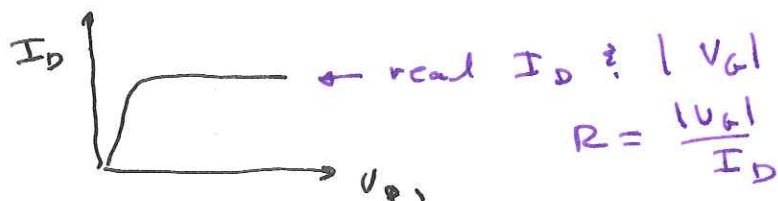
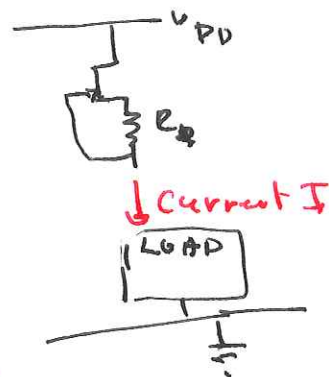




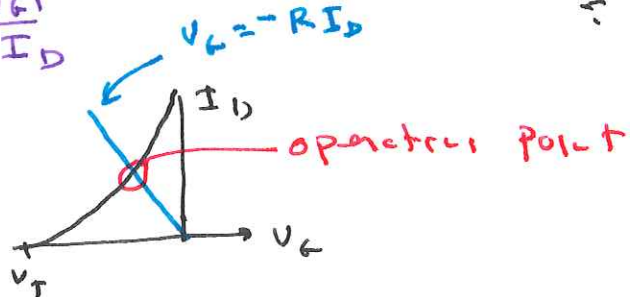
Repeat warnings: $R_D \rightarrow \infty$ is a bad idea

"Active Load" - HH talks about improving followers with active load that is a good & useful idea.

Good Idea: FET as a current source - set I via R . [Note: $R \rightarrow \infty \Rightarrow I_{DSS}$]



$$R = \frac{|V_{GS}|}{I_D}$$



alt: load line analysis:

Remark: HH talks about "current limited diodes" - pre built FETs with correct R to produce a specified current.

These always sound like a great idea to me, but any time I've thought to use them I've found them ① hard to find (buy eg. from Digi-Key) ② pricy - much more than a FET.

Good Idea - FET (in its linear region) is a voltage controlled resistor. The "linear region" is not super linear but HH describe how to improve it.

$$\frac{1}{R_{ps}} = \underbrace{2k}_{g} \left[(V_{GS} - V_T) - \frac{V_{DS}}{2} \right]$$

Good Idea - use a ON/OFF FET (particularly a MOSFET) as a switch.

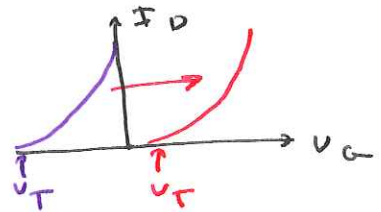
On resistance $\text{few } \Omega$; OFF: expo small leakage currents.

MOSFETS can control multiple As! - Power MOSFETS

packaged "analog switches"

enhancement mode MOSFET

2N7000: TTL signals control 100mA



Why use a discrete FET instead of a 411?

→ high input impedance → for followers

(FET amps don't have much gain; are subject to parameter variations)

→ current source

→ sometimes a single FET exactly matches need

→ MOSFET current switches / power control

↪ recall switching power supplies