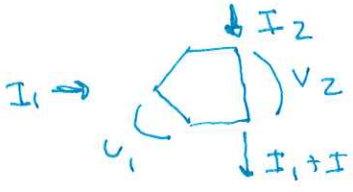
Small Signal Model — the superposition Thm allows us to totally separate signals at different frequencies. In particular we separate the DC signals (volt / amps) — which we call the 'bias' — from AC signals. We must assume the AC signals are 'small' so we can approximate nonlinear response with just the linear term of Taylor's approx. [Superposition required linear circuit elements]

Thus we consider a generic 3-terminal device



We assume currents are known functions of voltages. [There is nothing special about this — in future we'll consider cases where voltage is a function of current. On the other hand the range of validity of Taylor Approx may depend on what we take as dependent / independent variables — ie some models really are better than others]

$I_2(V_1,V_2)$: $dI_2 = \frac{\partial I_2}{\partial V_1} dV_1 + \frac{\partial I_2}{\partial V_2} dV_2$

$\frac{\partial I_2}{\partial V_1}$: transconductance g, forward admittance y_{fs}

$\frac{\partial I_2}{\partial V_2}$: output admittance $y_{os} = \frac{1}{R_o}$

$I_1(V_1,V_2)$: $dI_1 = \frac{\partial I_1}{\partial V_1} dV_1 + \frac{\partial I_1}{\partial V_2} dV_2$

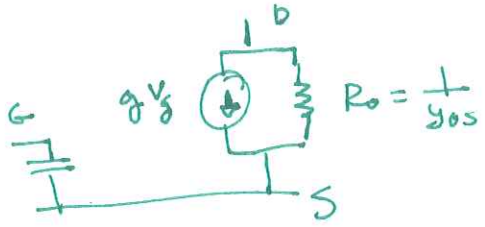
$\frac{\partial I_1}{\partial V_1}$: input admittance $y_{is} = \frac{1}{R_i}$

$\frac{\partial I_1}{\partial V_2}$: so small I've never seen a value for this

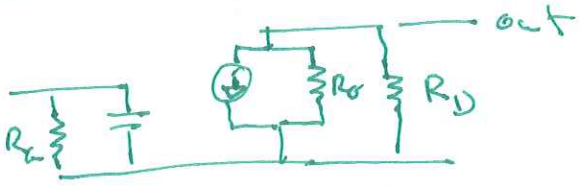
For FETs this term is truly small, bias dependent and hence not in spec sheet

Note: input capacitance is in spec sheet → $y_{os} = i\omega C$

Resulting model for FET:



AC model for common source amp:



so gain is now $g(R_o \| R_D)$

EE notation (which I will probably violate sometimes)

I_D - DC current into drain - cap symbol & subscript

i_d - AC current into drain - lowercase " "

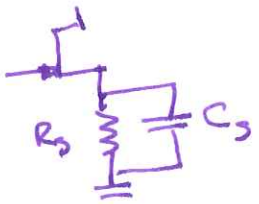
i_D - AC+DC current into drain - lowercase symbol uppercase subscript

eg (future) h_{FE} - ratio of 2 total currents

h_{fe} - ratio of just AC parts

Remark: Common Source Amp - rid $\frac{1}{t} V_G$ & $\frac{1}{t} R_G$ (maybe)

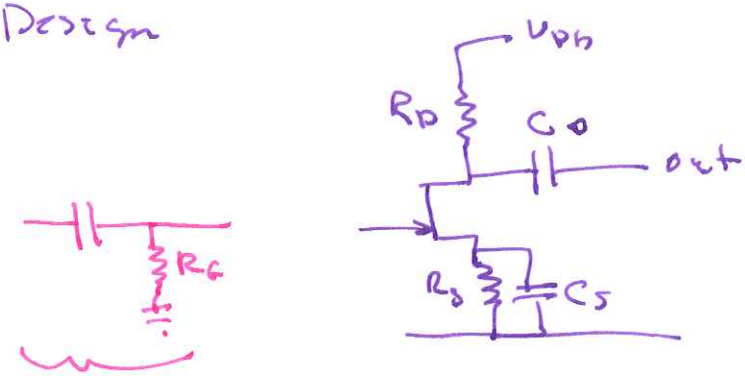
plan: have $V_G = 0V$ but $V_S = +1V$ (eg) so $V_{GS} = -1V$. Let V_S be steady even as I_S (i_S) varies.



select $R_S \Rightarrow I_D R_S$ = desired $|V_{GS}|$

select $C_S \Rightarrow \frac{1}{\omega C} \ll R_S$ for lowest desired freq.

Design



high pass filter blocking cap

Select Quiescent Point (aka Operating Point)

→ $V_{DS} \approx \frac{V_{DD}}{2}$

→ smaller I_D → bigger R_D

⇒ bigger gain but bigger output impedance

Given an operating point – Find R_S / C_S to supply the required bias

C_D: this cap will probably be connected to something with an R_{in}. Good practice requires that R_{in} to be big compared to circuits output impedance ($= R_D \,||\, \frac{1}{y_{os}}$) & generally $R_D << \frac{1}{y_{os}}$.

Thus we should be OK with $X_C = R_D$

[Solve for C using lowest interesting freq]