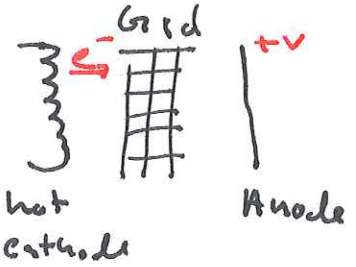
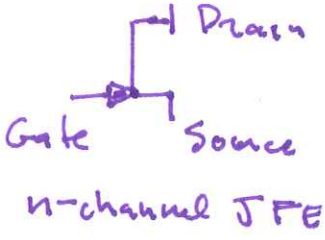
3 terminal devices — we start with the ancient triode [usually attributed to Lee deForest (1906) [PhD under Gibbs at Yale] but not much used until 1912]

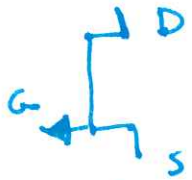


The flow of electrons cathode → anode can be affected (reduced) by putting a negative voltage on Grid. Note that Grid sits in vacuum — essentially disconnected — so basically zero current & hence zero power in. The mA scale cathode-anode current @ 100 V represents ~1W power so we have potential for power gain.

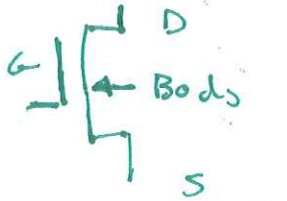
The physics of Field Effect Transistors (FET) is not much like a triode but the basic idea is the same — a voltage (at zero current) controls a larger current flowing between two other terminals



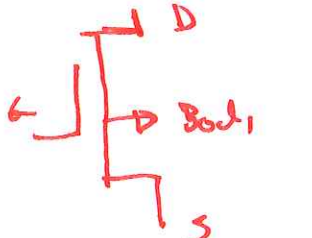
n-channel JFET



p-channel JFET

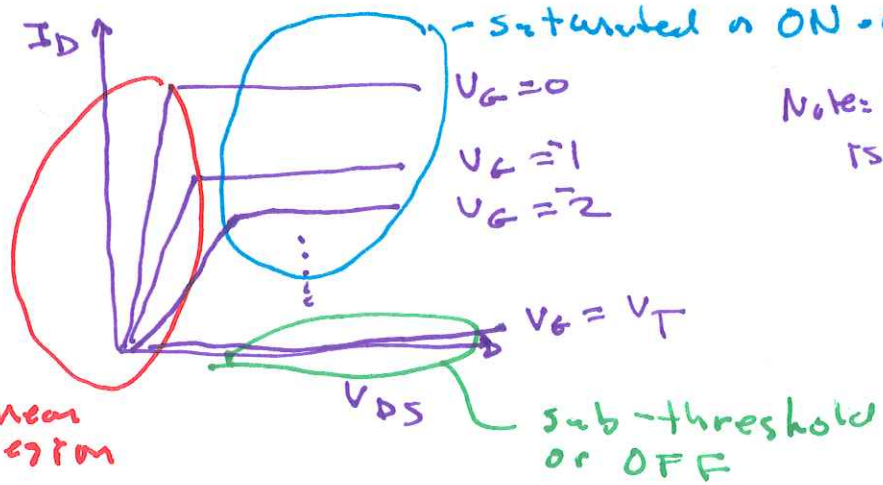


n-channel MOSFET



p-channel MOSFET

We display the behavior of these 3-terminal devices with characteristic curves — plots of I thru vs V across for various control voltages



- saturated = ON or ACTIVE

Note: term "pinched-off" is ambiguous — avoid

Currently we restrict consideration to the saturated regime where I_D plateaus (ie I_D is constant as V_{DS} increases — not like a resistor). There

$$I_D = k(V_G - V_T)^2$$

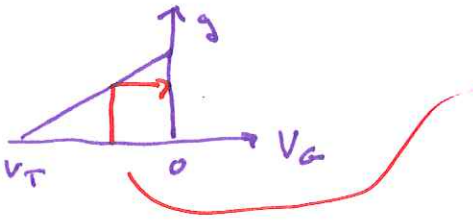
$V_G - V_T \equiv$ gate drive — larger means more current

↑ For n-channel JFET this is negative & V_G would also be negative, but $V_G - V_T > 0$

As shown below we will be interested in

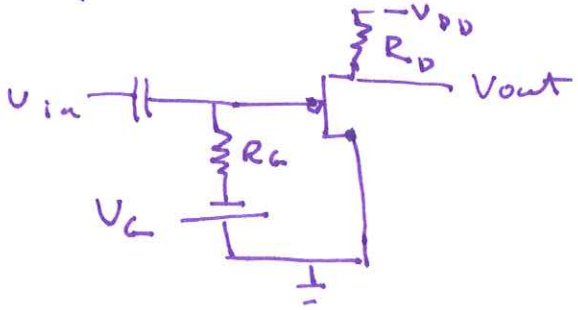
$$\frac{dI_D}{dV_G} = 2k(V_G - V_T) = g = g_{fs}$$

g ← transconductance; g_{fs} ← forward admittance



often we will be interested in g at a particular voltage — the operating point

Simple circuit - Common Source Amp

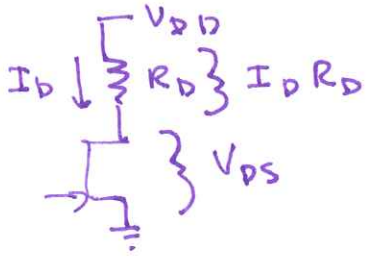


V_G is used to set a particular V_G. V_{in} will slightly modify that V_G [The capacitor is a bypass cap — V_{in} will appear with a DC offset]

$$V_{out} = V_{DD} - R_D I_D$$

$$\frac{dV_{out}}{dV_{in}} = -R_D \frac{dI_D}{dV_{in}} = -R_D g$$ ← inverting amp with a DC offset.

Load Line Analysis – plot the equation for R_D on top of the characteristic curves of FET.



$$V_{DS} + I_D R_D = V_{DD}$$

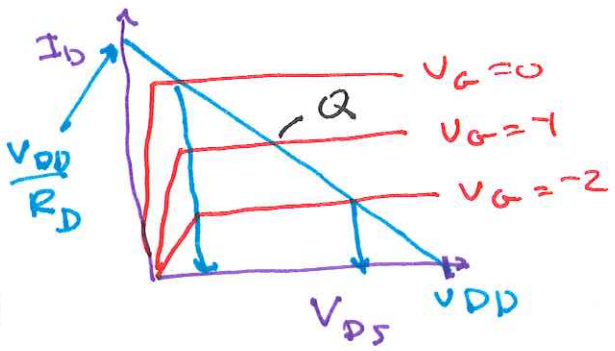
$$I_D = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$$

$\frac{V_{DD}}{R_D}$ ← y intercept (current that would flow if FET shorted out)

x intercept: if $I_D = 0 \rightarrow V_{DS} = V_{DD}$

Assume V_G set = −1 V by bottery. Quiescent Point Q. As V_{in} swings V_G ±1V (to 0→2)

V_{DS} also changes (inverted)



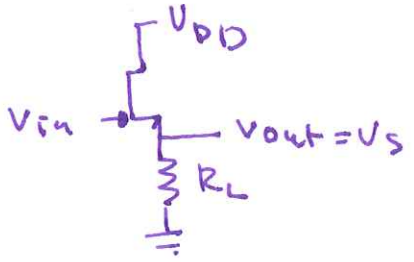
$$\Delta I_D = \underbrace{\frac{dI_D}{dV_G}}_{g} \Delta V_G = \left(-\frac{1}{R_D}\right) \Delta V_{DS} \rightarrow -g R_D = \frac{\Delta V_{DS}}{\Delta V_G}$$

In the above I've shown the characteristic curves as exactly flat – no change in I_D as increase V_{DS} – In fact some slope $\frac{\Delta I_D}{\Delta V_{DS}} = y_{os}$ "output admittance"

Output Impedance – "ground input" & apply extra voltage V to output. Reduces current thru R_D increases current thru FET: Must add current: $\frac{\Delta V}{R_D} + y_{os} \Delta V$

$$\frac{\Delta V}{I} = \frac{1}{\frac{1}{R_D} + y_{os}} \rightarrow R_D \parallel \frac{1}{y_{os}}$$

Source Follower



$$\Delta V_S = \Delta I_D R_L$$

$$= g \Delta (V_{in} - V_S) R_L$$

$$(1 + g R_L) \Delta V_S = g R_L \Delta V_{in}$$

$$\frac{\Delta V_S}{\Delta V_{in}} = \frac{g R_L}{1 + g R_L} \approx 1$$

Output Impedance: Force V_{out} up by V

increase in current thru $R_L = \frac{V}{R_L}$

decrease in current thru FET $= -g V$

I = total added current $= \left(g + \frac{1}{R_L}\right) V$

$\frac{1}{g + \frac{1}{R_L}} = \frac{V}{I} = R_{out} \rightarrow \frac{1}{g} \parallel R_L$ ← 300Ω