Physics 217A LAB 2 Spring 2016

Decoders, Latches and JK Flip-Flops
Switch Bouncing and Tri-State Logic

Part I

0. This part requires about 45 connecting wires! The first part of this lab leads, step-by-step, to the production of a multi-chip circuit that might be interfaced to a computer. The circuit action begins with the decoding of a three-bit address. When the address is 1–3, the circuit lights an appropriate LED. When the address is 4–7, nothing happens. (In practice, these addresses would be used to enable other actions, as with address 0.) When the address is 0, the decoder enables a four-bit latch, unfreezing its outputs, which now follow the data on four data lines (supplied by four side-board switches). The output of the latch is fed into a seven-segment decoder, which in turn displays the data on a seven-segment display. You will build the circuit backwards, checking if each chip works before you go on to the next stage.

1. Press in the following TTL chips (from top to bottom): 74138 (octal decoder), 7404 (hex inverter), 7475 (four-bit latch), 7448 (seven-segment decoder); leave room on the very bottom for the seven segment display. Every chip, except the 7475, takes power and ground "at the corners." Power-up the TTL chips. Press in a (common cathode) seven-segment display. Ground the common cathodes. *Do not hook any display pin directly to +5 V — that results in immediate destruction of a segment!*

2. Use a 1 kΩ to 3 kΩ resistor and hook it between +5 V and a empty row of holes. Attach one end of a wire to a hole in the row. Briefly attach the other end of the wire to hole connected to a 7-segment anode pin, and check to see that the segment lights up. (Segments are diodes; when forward-biased with +5 V they conduct too much current and are destroyed in a quick fizzle. The resistor limits the current to $(V_{CC} - V_{\text{diode}})/R$, i.e., a few milliamps.)

3. Hook up the four inputs of the 7448 to four (side board) data switches. (Note the '48 inputs a parallel binary number in the form: MSB=D,C,B,A=LSB.) Hook up the segment-driving outputs to the correct display segment. Check to see that BCD data are correctly displayed. Record in your notebook the display when the data switches produce values 10 through 15.

4. Move your data switch wires from the 7448 to the "D" inputs of the latch. Connect the enable pins together and to a fifth data switch. Connect the "Q" latch outputs to LEDs. Note the transparent latch action: Q follows D, if the latch is enabled; Q holds its value, independent of D, if not enabled.

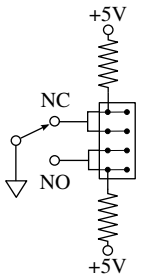
5. Move your latch outputs from the LEDs to the correct 7448 inputs. Check that the latching, displaying action works correctly.

6. Connect up your three remaining data switches to the 74138 decoder address lines. Ground pins 4 and 5 to enable the '138. Feed outputs 0–3 through inverters to LEDs. (Note that the '138, like most decoders, is "active low", i.e., a normally high output is sent low when selected — hence the need for an external inverter to light an LED when selected.) Give several examples of the decoding action.

7. Use the externally inverted, 0-address output to enable the latch. Display the working circuit to your instructor. Done.

Part II

0. In this part you wire up an old pulse-clocked JK FF and an LS edge-triggered JK FF, and compare the two. You also see an example of tri-state logic and investigate switch debouncing. You will be using the easy-to-destroy debounced pushbutton as a clean clock. Recall that these are open collector (see HH 10.2.4.C) devices and require a $\sim$3 kΩ "pull-up" resistor which you should supply. Today you will be using the NC (normally connected) end, so you need only supply a pull-up resistor to that connection. Recall: never make a direct power supply connection to these pushbuttons.



1. Press in and power up a 74LS107 and 7473 (not LS!). Note that the '107 takes power at the corners, while the '73 uses the second most common power/ground pinout. For both devices, wire 1CLR, 1J, 1K to data switches, 1Q to a LED, 1CK to a NC (normally connected) debounced pushbutton. Display the debounced pushbutton's output on an LED. Clock both JKs with the same pushbutton. Check out the truth table. Record in your notebook (using words not symbols) the truth table of the JKs. What sort of edge triggers these JKs? Does this happen when you press the pushbutton or release the pushbutton? Explain (words) why this is the case.

2. Now use the '107 output to clock the '73. Carefully record in your notebook (a vertical stack of three graphs (CK, '107 Q, '73 Q) works best) the results as you clock the daisy chain when both the '107 and the '73 are in toggle mode. Your sketch should show both outputs and the clock input. (See HH Fig. 10.71)

3. Move the clock input for the '107 from the pushbutton to a data switch. Note (record) an example of unreliable results. This is because of switch bounce. (See HH p. 729–30)

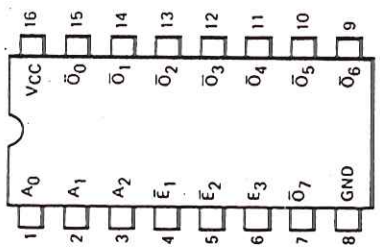
4. There is a standard 4000 series CMOS IC that can provide the SR latches needed for switch debouncing: 4044. Press in and power up (at the corners) this IC. Route the tri-state enable, pin 5, to a data switch. Wire in a SPDT switch with ground on the pole and with each throw connected via a $\sim$3 kΩ pull-up resistor to +5 V. (See HH Fig. 10.51 also on pin-out pages of this manual) Connect one throw to R1 and the other to S1. See that the two switch positions correspond to (S,R)=(0,1) or (1,0); inbetween the switch positions (S,R)=(1,1).

5. Use the output of the debounced switch to clock the daisy chain of JKs. Note that the bouncy switch is debounced; reliable clocking is the proof.

6. Check out the Hi-Z output state ("OC", see HH p. 720) present when tri-state enable is low. Measure the current and voltage resulting from a "wired or" between a JK output and a 4044 output in the Hi-Z state. (The circuit should be just output-to-output, with no additional wires sending power to other devices like LEDs. Note: wired-or is generally a huge no-no.) As the JK output changes state, does the "wired or" voltage follow appropriately? (The easy way to change the JK output state is to change the circuit: connect to $\overline{Q}$ rather than Q.) How much current flows? These measurements should show that a pin in a Hi-Z state acts exactly like a disconnected pin (i.e., an open circuit).

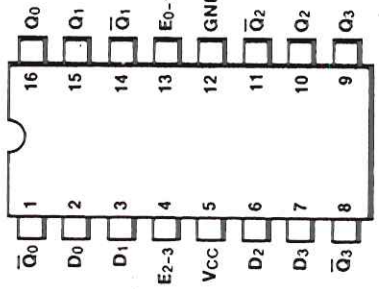
7. Note that in the above we have connected a CMOS output (from the 4044) to a TTL LS input (on the 74LS107). Connecting different logic families can cause problems (see HH 12.1.3). Try clocking the 7473 with the 4044 output. If that works, try fanning out the 4044 output to feed both 7473 clock inputs. The larger current loads (in the low state) of (1) 74XX vs. 74LSXX or (2) large fan-out generally complicates interconnection of CMOS $\rightarrow$ TTL.

74138

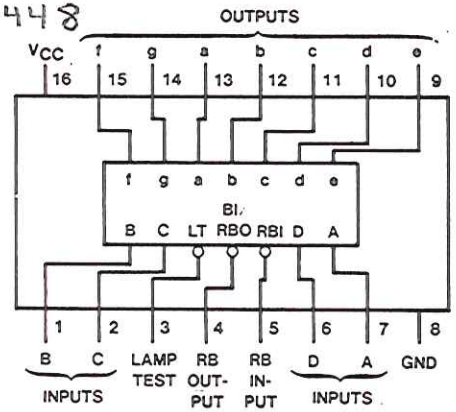


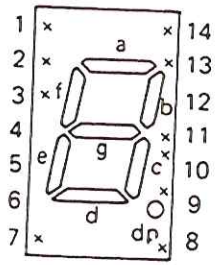
7475

54LS/75LS75

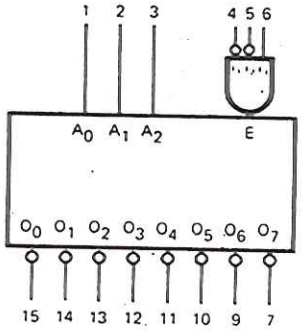


7448





Pin No.	LN514RK, LN514GK, LN514YK, LN514OK
1	Anode a
2	Anode f
3	Common Cathode
4	–
5	–
6	–
7	Anode e
8	Anode d
9	Anode dp
10	Anode c
11	Anode g
12	–
13	Anode b
14	Common Cathode



PIN NAMES

D_1–D_4	Data Inputs
$\overline{E}_{0-1}$	Enable Input Latches 0, 1
$\overline{E}_{2-3}$	Enable Input Latches 2, 3
Q_1–Q_4	Latch Outputs (Note b)
$\overline{Q}_1$–$\overline{Q}_4$	Complimentary Latch Outputs (Note b)

48, LS48

Decimal or Function	Inputs LT	RBI	D	C	B	A	BI/RBO(1)	Outputs a	b	c	d	e	f	g	Note
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	(2)
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	(3)
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	(4)
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	(5)

Note 1: BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

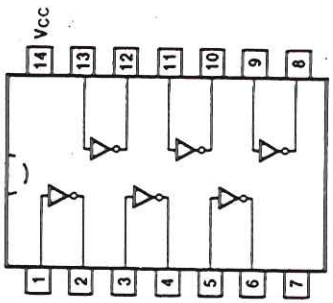
Note 2: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired

Note 3: When a low logic level is applied directly to the blanking input (BI), all segment outputs are H (46, 47); L (48) regardless of the level of any other input.

Note 4: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).

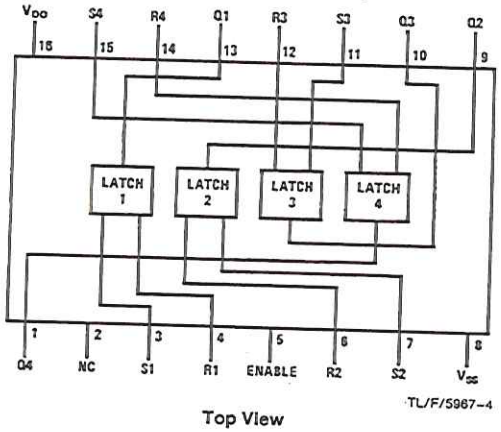
Note 5: When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L.

H = High level, L = Low level, X = Don't Care



7404

CD4044BM/CD4044BC
Dual-In-Line and Flat Packages



TL/F/5987–4

Top View

Order Number CD4043B or CD4044B

OC — TRI-STATE
NC — No change
X — Don't care
Δ — Dominated by S = 1 input
ΔΔ — Dominated by R = 0 input

CD4044BM/CD4044BC

S	R	E	Q
X	X	0	OC
1	1	1	NC
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

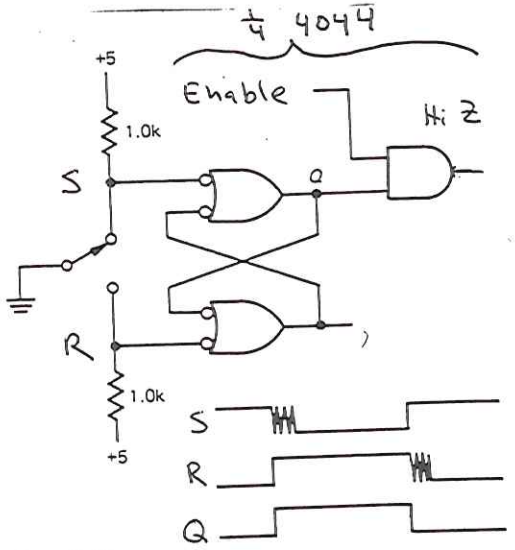
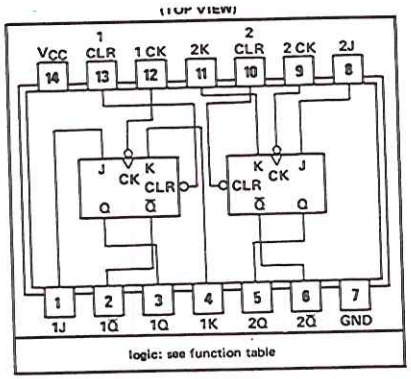


Figure 8.42

107



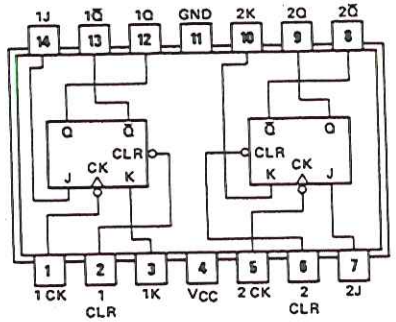
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

J K FF

73



'73, 'H73, 'L73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\bar{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	