Programmable chips – chips whose function can be changed by user after purchase – "burn in" a function forever or modify on-the-fly in a few ns.

ROM (Read Only Memory) – an address selects a particular item which might be a bit or byte of binary output

PROM (programmable – burned)

EPROM (uv erasable)

EEPROM (electrical erasable)

flash

Note: can be used to implement a truth table via look up table but slower than gates

RAM – Random Access Memory

DRAM – dynamic – requires refresh

SRAM – static

PAL, PLA (programmable logic array)

"burn in" a minterm expression – a 1 chip solution

FPGA (field programmable gate array)

generally more complex & expensive than PALs incorporates clocked registers and even CPU beyond (but includes) Combinational logic to sequential logic

CPU – (central processing unit)

instructions update registers and are designed to store/load to/from RAM. Instructions stored in a block of RAM indexed by PC (program counter). Note stack pointer (SP) and other addressing modes.

Addressing modes — (R) denotes contents of R

register R : (R) is operand

deferred (R) : (R) is address of operand

auto increment (R)+ : (R) is address and (R) incremented

auto decrement -(R) : (R) is decremented and used as address

combine to make a stack pointer (SP) push pop

index X(R) : address is X (a supplied value) + (R)

immediate : actual value supplied in instruction

absolute/direct : address given as part of instruction

PC relative : good for position independent code.

Note: names & notations vary from CPU to CPU

Note: RISC (reduced instruction set computers)
CISC (complex instruction set computers)

Key Fact: RAM is slow compared to registers
Try to help with cache memory of intermediate speed.