Synchronous Counter: $0 \to 1 \to 2 \cdots \to 6 \to 7$ (back to 0)

count: 3 bit binary number ABC

"synchronous" requires same clock for all

plan: let present state determine future via gates

current A B C	Future D_2 D_1 D_0
0 0 0	0 0 1
0 0 1	0 1 0
0 1 0	0 1 1
0 1 1	1 0 0
1 0 0	1 0 1
1 0 1	1 1 0
1 1 0	1 1 1
1 1 1	0 0 0

D_0	A \ BC	00	01	11	10
	0	1	0	0	1
	1	1	0	0	1

$D_0 = \bar{C}$

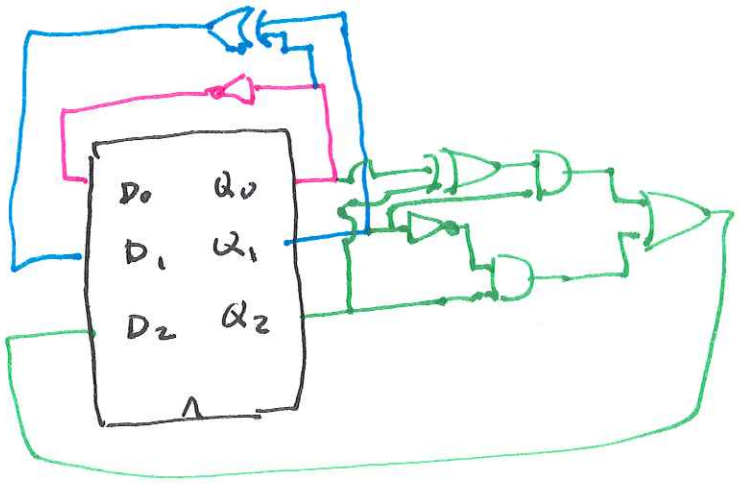
D_1	A \ BC	00	01	11	10
	0	0	1	0	1
	1	0	1	0	1

$D_1 = \bar{B}C + B\bar{C}$

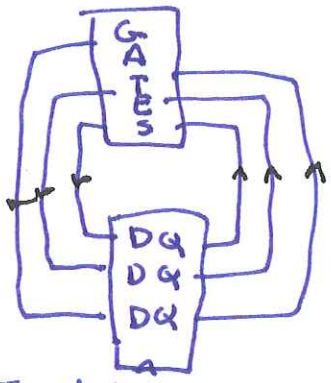
$= B \oplus C$

D_2	A \ BC	00	01	11	10
	0	0	0	1	0
	1	1	1	0	0

$D_2 = A\bar{B} + B(A \oplus C)$



Note general ideal



GATES determines next step from current

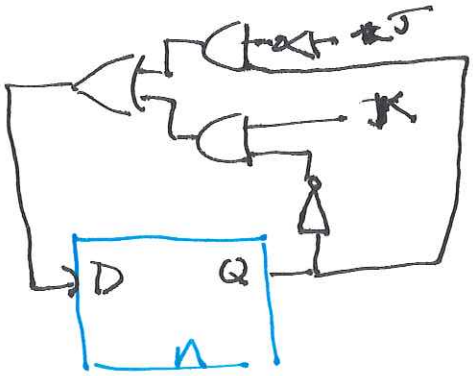
Make JKFF from DFF

(add external controls JK to GATES)

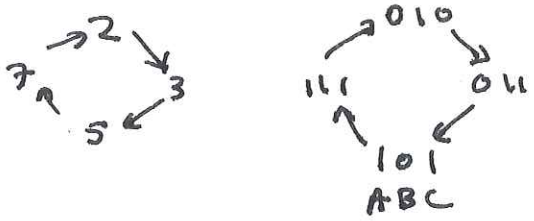
J K Q	D	
0 0 0	0	hold
0 0 1	1	
0 1 0	0	clear
0 1 1	0	
1 0 0	1	set
1 0 1	1	
1 1 0	1	toggle
1 1 1	0	

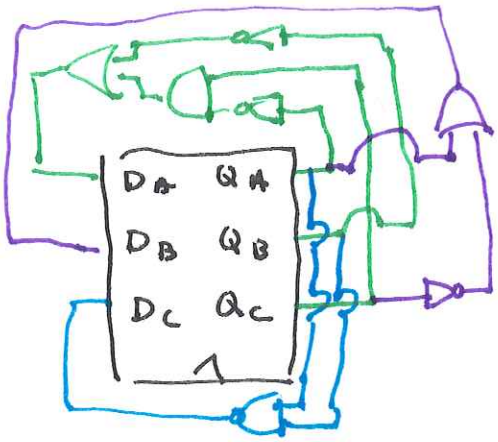
D	Q \ JK	00	01	11	10
	0	0	0	1	1
	1	1	0	0	1

$D = K\bar{Q} + \bar{J}Q$



State Diagram for prime number counter





C \ AB	00	01	11	10
0	X	3	X	X
1	X	5	2	7

B:t0

	00	01	11	10
0	X	1	X	X
1	X	1	0	1

$\bar{A} + \bar{B}$ = $\overline{AB}$

B:t1

	00	01	11	10
0	X	1	X	X
1	X	0	1	1

$A + \bar{C}$

B:t2

	00	01	11	10
0	X	0	X	X
1	X	1	0	1

$\bar{B} + C\bar{A}$

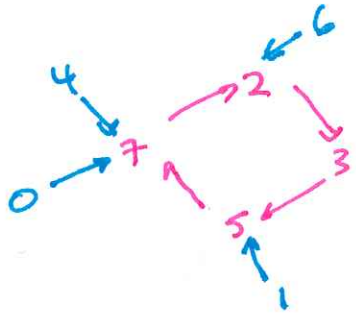
$D_A = \bar{B} + C\bar{A}$

$D_B = A + \bar{C}$

$D_C = \overline{A \cdot B}$

0	1	1	0		1	1	1	0
1	0	1	1		1	0	0	1
1	1	1	0		1	1	1	0
↑	↑	↑	↑		↑	↑	↑	↑
2	3	5	7		0	1	4	6

check — exclude states



Worry: a state that does not return to cycle.

if $D_A = \bar{B} + A \oplus C$

then for 6 $D_A = 1$ so

New general problem: given any state diagram produce a circuit that follows it.